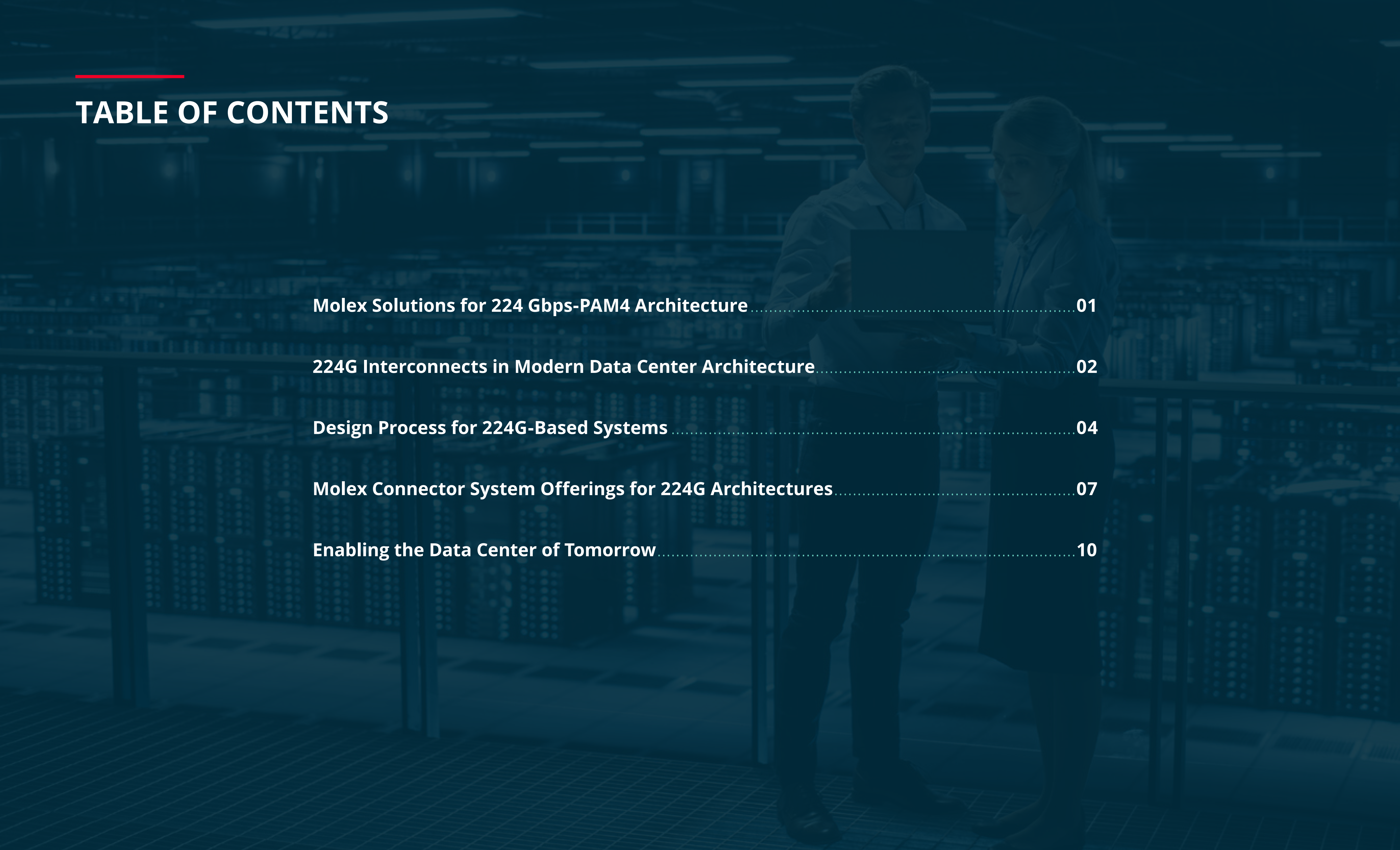
SOLUTION GUIDE

Building the Next-Gen Data Center with 224 Gbps-PAM4 Technologies

molex



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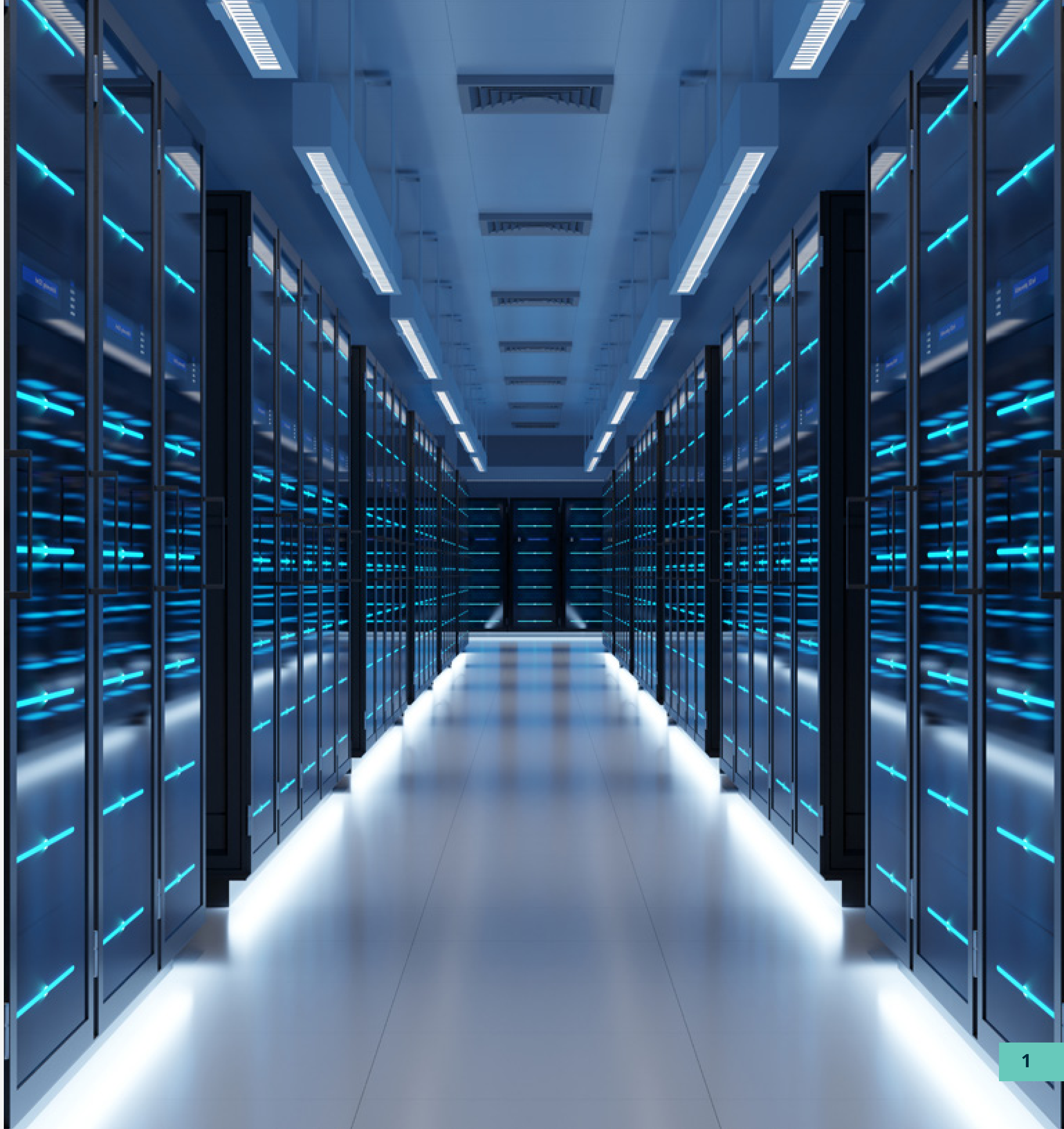
MOLEX SOLUTIONS FOR 224 Gbps-PAM4 ARCHITECTURE

Each generation of high-speed serial communication has pushed channel data rates to progressively higher levels, and each new bandwidth requirement stretches the limits of signal integrity through an interconnect. Engineers have exploited numerous tricks to continue extending channel bandwidths past a bitstream's Nyquist frequency, but systems running at 224G also need component solutions that can support these ever-higher channel bandwidths.

When we look in the data center, 224G channels span from ASICs, across printed circuit boards (PCBs) and backplanes, through connectors, through passive and active cables and through optical fiber so that networking and compute equipment can communicate with each other. Without connector and cable systems, these channels could not exist outside of silicon and at short distances in a PCB.

To ensure a system performs as designed, proper channel modeling and simulation during component selection is critical. In this guide, we review the design considerations, associated challenges and solutions to the next generation of data center architecture built for 224G — and how Molex matches solutions to performance requirements, provides signal integrity data and brings valuable insight starting on day one.



224G INTERCONNECTS IN MODERN DATA CENTER ARCHITECTURE

Although a 224G solution will be specific to the application, a typical fabric and scale out architecture can be visualized to trace a signal through a system — highlighting the role of connectors along the way. As shown in the block diagram in Figure 1, signals originate and are received in a processor unit (CPU, GPU, TPU, etc.) and travel through a BGA (ball grid array) pattern (BGA1) and through a PCB. A near-chip connector receives these signals and transfers them along a hybrid cable, moving through a high-density backplane connection, and subsequently through an external backplane cable, forming a fabric channel.

Signals then take the forward journey from BGA2's land pattern into another near-chip connector, to the front panel I/O connector using a BiPass cable, and eventually out into a passive or active copper cable or fiber interconnect. Data is then sent to another unit in the data center and used in a larger application.

Within this architecture, there are multiple points where connectors play a critical role in 224G channels: near or at ASICs, the backplane cable interface, the BiPass cable interface, on the fabric channels and on the scale out channels.

A TYPICAL ARCHITECTURE HIGHLIGHTS THE CRITICAL ROLE FOR 224G CONNECTORS

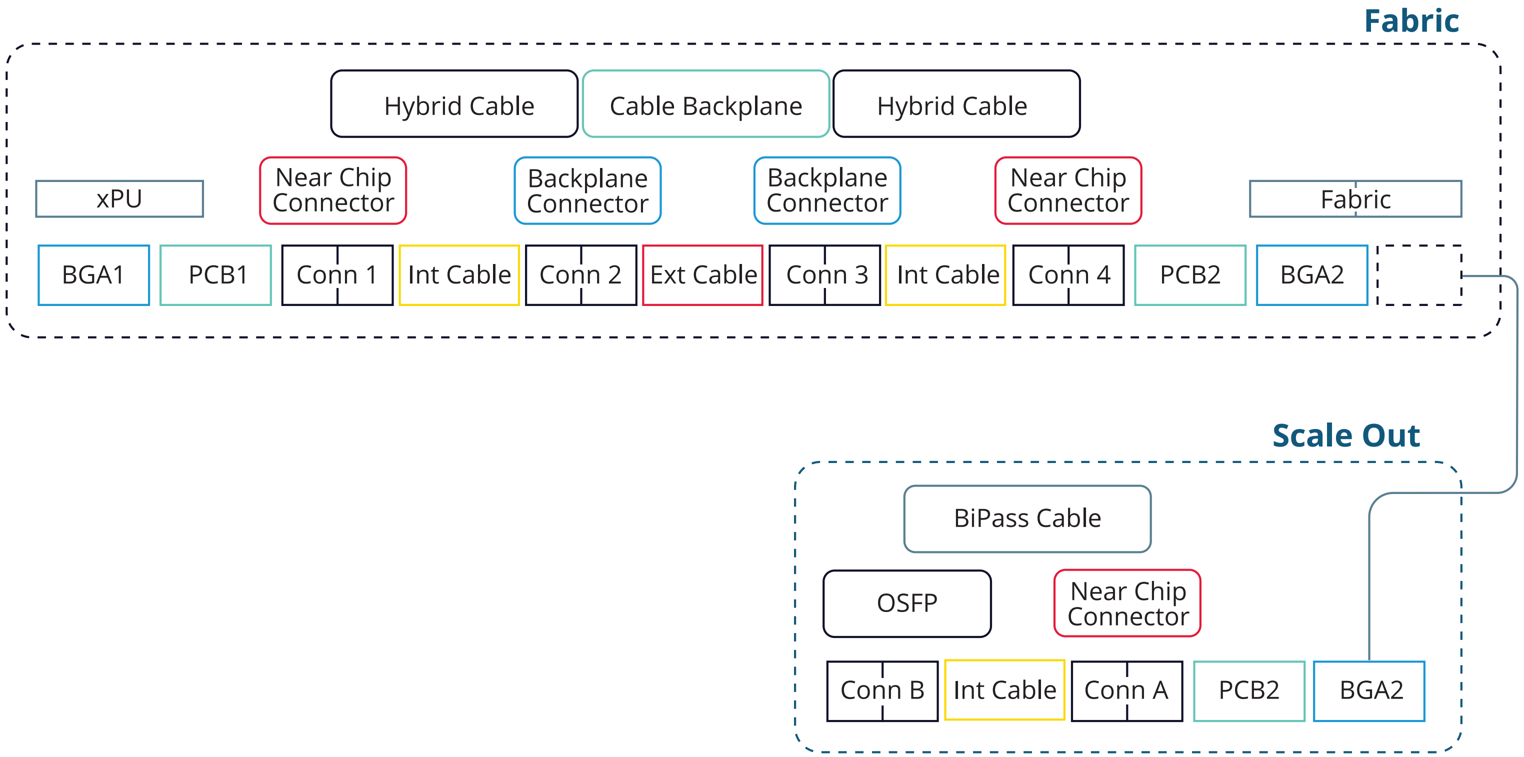
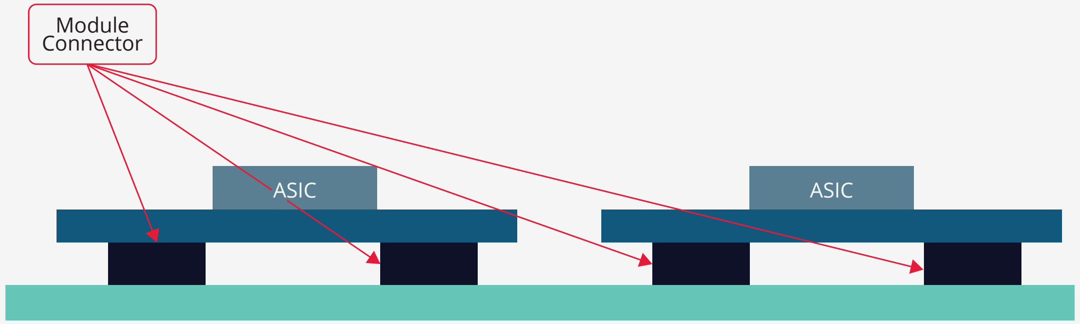


Figure 1: *Block Diagram of Fabric and Scale Out Architecture*



CONNECTORS IN FABRIC CHANNELS

The fabric channel operating in a data center environment is increasingly constructed with cable, and more and more often, backplane cable. This is made up of a cable and connector system that enables high speed data transfer between modules connected to the backplane, giving access to servers or infrastructure equipment. The specialized cabling used in backplane cables offers lower loss and provides longer interconnect reach than 224G traces on a PCB, enabling designers to consider architectures that might not be achievable without their use.

CONNECTORS IN SCALE OUT CHANNELS

Copper or optical cables coming into the system transition into the PCB via a standardized high-speed copper connector such as a quad small form factor pluggable double density (QSFP-DD) or octal small form factor pluggable (OSFP) connector. Another flying lead cable connects back to a near-chip connector to transfer signals directly into or near an ASIC or processor package. From here, the embedded application can transfer data back along the fabric channel or into the scale out channel.

MODULE CONNECTORS FOR ASICs

While the BGA continues to remain the prominent connection mechanism between ASICs or processors and the PCB, some ASICs are placed on the PCB as modules. These modules require a board-to-board or mezzanine connector system such that signals from the ASIC can pass from the package substrate and into copper interconnects on the PCB.

These connectors can provide a simplified interconnect option directly into ASIC packaging that does not require precise design of a wideband signal launch in the BGA land pattern. These specialized land patterns can require 3D electromagnetic simulations for full qualification in the PCB, but an off-the-shelf option eliminates this design effort.

DESIGN PROCESS FOR 224G-BASED SYSTEMS

When 112 Gbps-PAM4 signaling was introduced into the data center environment, it was a major step beyond 56 Gbps-PAM4 signaling, doubling data rates through a doubling of interconnect bandwidth. Operating at 224G is not as simple as doubling the bandwidth for a transmitting component; these systems demand upgrades in the physical layer architecture to provide the required increase in bandwidth. This means all parts of the system are candidates for redesigns, including connectors and cable systems, and even down to the basic materials used to build PCBs and semiconductors.

To design systems operating with 224G channels, designers must balance the signal integrity requirements of each component in the architecture with the mechanical form factor requirements. Form factor is very important when selecting connectors and cabling due to the space constraints in data center environments. However, not all form factors and connector products will support 224G signaling, so designers must determine whether to prioritize signal integrity or mechanical form factor when evaluating components.

Table 1 demonstrates some of the factors found in 224G systems that influence signal integrity.

Connector interfaces	• Connector interface, attached cable and land pattern defines input impedance looking into the connector • Physical structure determines pin-to-pin crosstalk and emissions from the connector body
Chip I/Os	• Load capacitance and package inductance looking into the I/O pins can affect SI • Chip land patterns going into a PCB or module connector must be wideband to support 224G
Circuit board	• The circuit board can produce capacitive loading along a transmission line through parasitic capacitance
Copper transmission lines	• Copper roughness losses dominate at mid-range frequencies (below and near Nyquist) • Dielectric losses dominate at high frequencies (near and above Nyquist) • Differential crosstalk must sit below some limit up to Nyquist (-40 dB typical)

Table 1: *Influencers of Signal Integrity in 224G Channels*

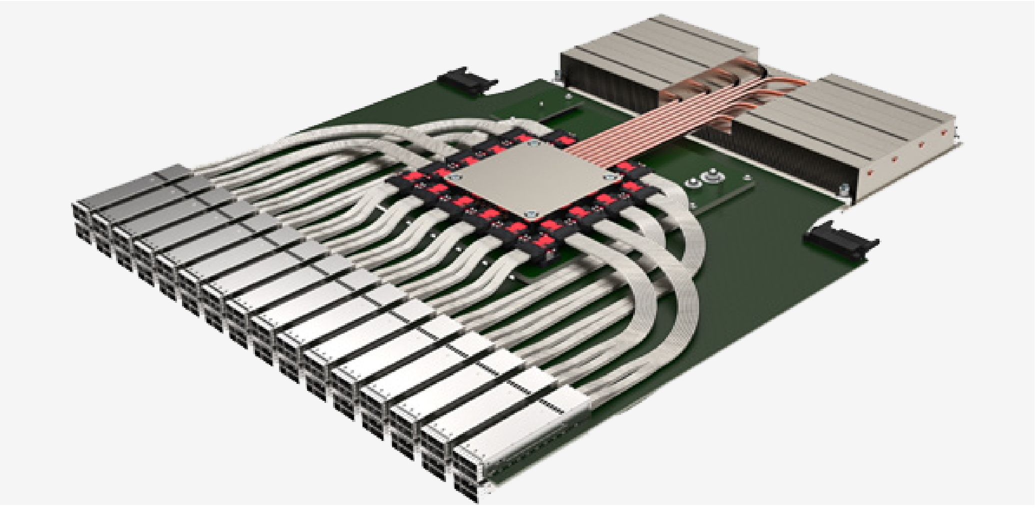
The best way to qualifying a design while prioritizing signal integrity is to take a system-level modeling approach with S-parameter models for the candidate connector products. Although a candidate connector may be rated for 224G, any of the factors shown in Table 1 could impact performance and lead to channel non-compliance. The connector provider can provide guidance on extracting connector models from simulation or capturing S-parameter data from measurement, or they can provide qualified data for use in simulations.

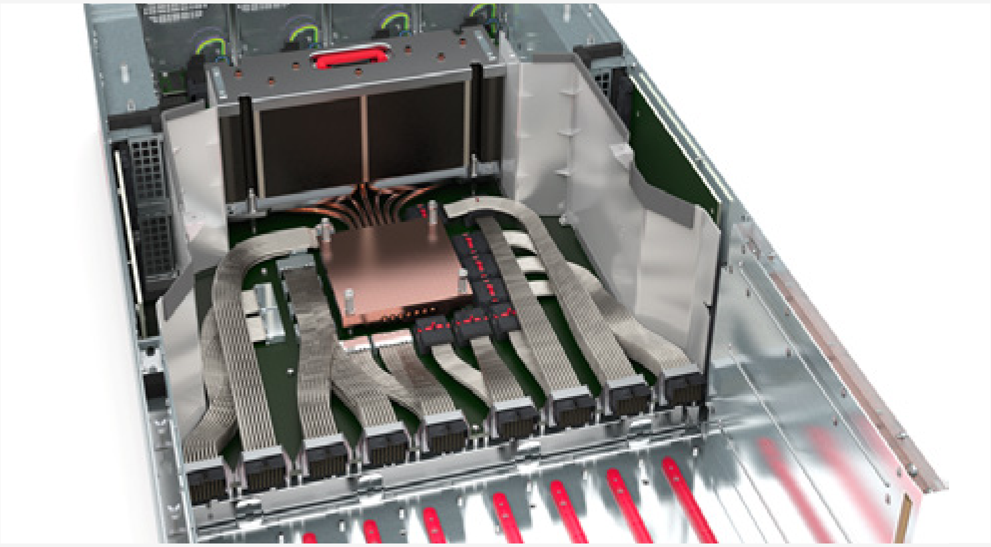
Within the set of design factors, designers have several methods they can utilize to push system bandwidths beyond 56 GHz and thus provide 224 Gbps-PAM4 connectivity. These include the materials used to build circuit boards, transmission line design and the connectors selected to enable 224G connectivity. In fact, connectors and cables are some of the most critical components influencing signal integrity in 224G channels – putting an even greater importance on partnering with a trusted and innovative connector provider.

CHIP I/Os AND PACKAGING

While systems designers can have ultimate control of aspects such as the PCB, cable implementation in the architecture and cable-to-board connector interfaces, some aspects of the system are not always within the system engineer's purview. This is particularly important when we look at packaging for the system host processor. Access to chip I/Os with minimal parasitics and reliable termination beyond Nyquist is the responsibility of the semiconductor/packaging provider, so this often represents a limiting factor that defines the loss budget along an interconnect.

Information about the chip and its packaging is important for modeling system behavior and determining whether other portions of the system can meet operational targets. Due to the short length of copper interconnects on a PCB in 224G channels, a significant portion of a signal's power spectrum interacts with the connector. A complete set of data should be selected when modeling system behavior.





PRINTED CIRCUIT BOARD (PCB)

The PCB allows mounting of chips and connectors such that signals can transmit between these elements. Vias in a PCB are highly capacitive at high frequencies for 224G channels, which can result in a reduction of interconnect impedance on the PCB. Due to the lossy nature of PCB interconnects, printed 224G channels tend to be rather short and utilized primarily for interfacing chips (either from BGA lands or module connectors) to wire-to-board connectors or fiber transceivers.

Shorter channels on a PCB will be return loss dominated, which requires precise impedance matching at each end of the printed interconnect. This means input impedance looking into connector bodies and chip packaging must be flat beyond the Nyquist frequency for a 224G channel to keep return loss low. When selecting a copper wire-to-board connector (such as twinax), the connector provider should specify the product's compliance with 224G requirements, as well as applicable signal integrity modeling data (e.g. in a touchstone file) for system-level simulation.

CABLE

Copper cable used in 224G architectures is appropriate for channel reach due to conductor losses in the cabling. While copper cable is lossy, advanced cabling types such as twinax can provide significantly less loss than PCB traces on low-loss dielectrics, making copper preferred in certain instances. The structure of twinax cable also ensures differential impedance can be maintained along the length of cable sections, which reduces return loss at connector interfaces.

When longer than 1m reach is needed or when the loss budget along the interconnect is low, an alternative to passive copper may be necessary. In such cases, active copper cable (ACC) or active electrical cable (AEC) can be used, which offers a lower cost option compared to optical cables to complete the interconnect link. In cable runs longer than 3 to 5m, where the link loss on passive or active copper will be much greater than the loss budget, signals can be routed into a fiber transceiver and are output over fiber optic cable. OSFP and QSFP-DD transceiver form factors are normally used for these interconnects, and these will appear in the scale out portion of the system architecture.

FORM-FACTOR-FIRST APPROACH

The other approach to designing systems with 224G channels is to select suitably rated connectors based on form factor. Aggressive designs in edge computing and artificial intelligence (AI) may prioritize small form factors, which will drive selection of connectors early in the design process. Following selection of connectors, signal integrity throughout the remainder of the system is optimized to ensure channel compliance.

One challenge in selecting connectors based on form factor is varying levels of standardization. In particular, interconnect solutions capable of supporting 224G are not universally standardized. While front panel I/O connectors in the scale out portion of the system architecture do have standardized form factors and cage options, connectors and cables come as systems that are not always interoperable between providers. This is a critical consideration when selecting and working with a connector provider early in the process to ensure the deployed system is extensible and scalable.

MOLEX CONNECTOR SYSTEM OFFERINGS FOR 224G ARCHITECTURES

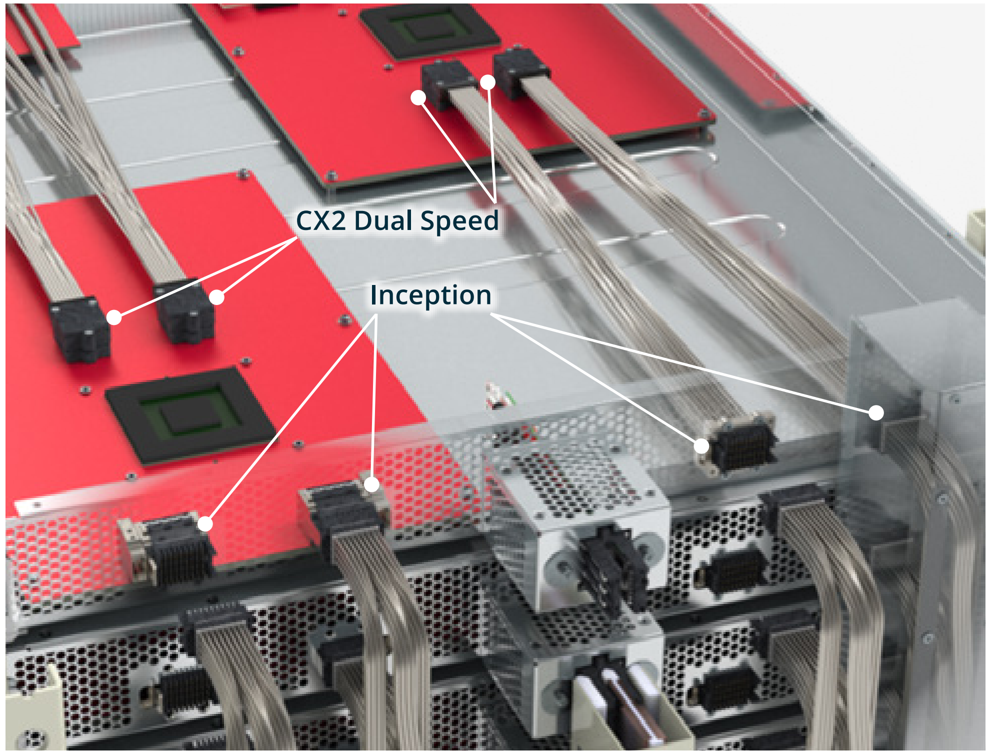
As a leader in next-generation data center architecture, Molex is first-to-market with a complete portfolio of 224 Gbps-PAM4 interconnect solutions. These products target all aspects of system architecture, ranging from ASIC interconnect solutions to cables and backplanes.

INCEPTION GENDERLESS BACKPLANE AND CX2 DUAL SPEED NEAR-ASIC CONNECTOR-TO-CABLE

Inception is an innovative genderless backplane system that prioritizes cable connections, providing the most flexible high-speed cable design within and between rack hardware architectures with hermaphroditic signal and mechanical integrity in the mating interface. As the backbone of the hardware communication architecture, Inception is designed for efficient communication and data exchange, and features a mechanically robust interconnect with the lowest loss cable tailored to fit into the tightest possible volume.

To complete the fabric, Inception can be paired with CX2 Dual Speed (CX2-DS), a near-ASIC connector and cable system, for high-speed, low-loss communication between the chip and surrounding components or external connection. CX2-DS connectors are designed for mechanical robustness, featuring screw engagement after mating to ensure full seating while transferring mating force to the screws, a reliable mechanical wipe and a fully protected, thumb-proof mating interface. Further, high performance twinax and an innovative shielding structure provide superior Tx/Rx isolation.

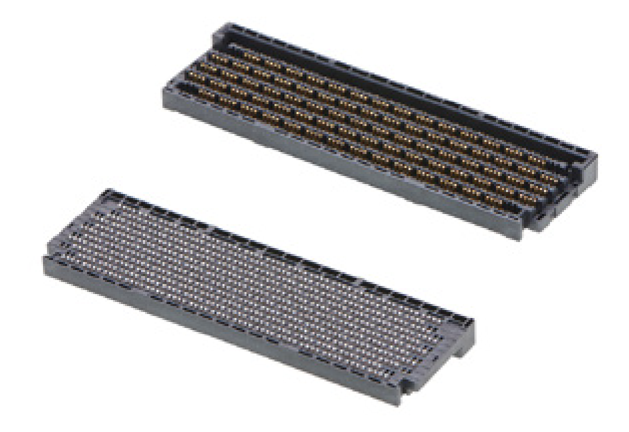
Combined, the components of the Inception and CX2-DS families provide a means of box-to-box scale up by interconnecting multiple chassis through 2-connector cable backplanes and 3-connector and 4-connector systems — each optimized for speed and mechanical robustness.

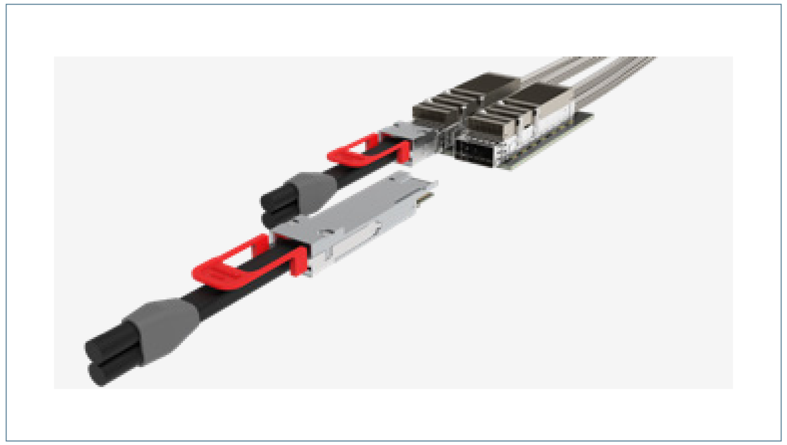


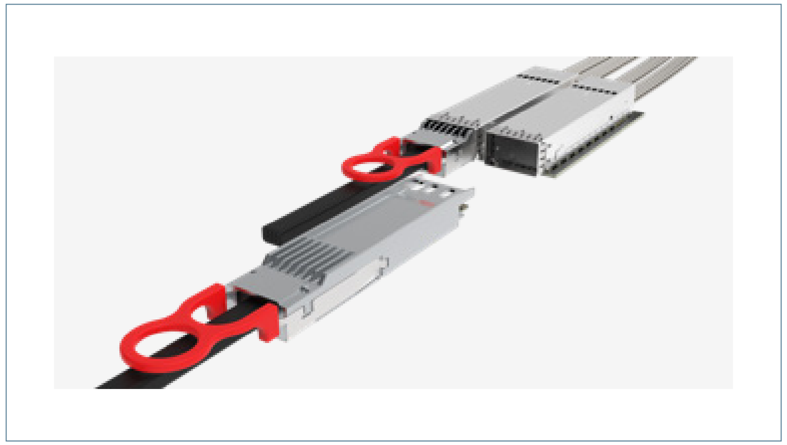
MIRROR MEZZ ENHANCED 224G BOARD-TO-BOARD CONNECTOR

Mirror Mezz Enhanced brings our mezzanine interconnect technology to a level capable of supporting 224 Gbps-PAM4. We have improved impedance tolerances and crosstalk compared to previous versions while maintaining an industry-leading density down to a 5mm board-to-board height. Mirror Mezz Enhanced also maintains the hermaphroditic nature and form factor of the Mirror Mezz line to reduce stock keeping unit (SKU) count on the system bill of materials (BOM).

Designed for modularity, individual compute modules can be added or removed to tailor each chassis to a desired capability level. By adding more Mirror Mezz Enhanced connections to a system, as well as the supporting topology on the PCBA, a system can support additional compute modules, facilitating the incremental scale up of compute power. A great example of this in the market today is the OCP Open Accelerator Infrastructure (OAI) system which can support up to 8 GPU modules if fully populated. In future architectures, such as described above, a system like the OAI, when used in conjunction with the Inception/CX2 Dual Speed interconnection fabric, can also connect between separate chassis using backplane connectors and cables.







OSFP 1600, QSFP 800 AND QSFP-DD 1600 CONNECTOR AND CABLE SOLUTIONS

Built for 224 Gbps-PAM4, these robust I/O connectors and cables offer superior mechanical durability and excellent shielding to minimize crosstalk and deliver better signal integrity performance at a higher Nyquist frequency.

OSFP 1600 is the next generation upgrade of our OSFP product family and is MSA compatible for 224 Gbps applications. When backwards compatibly with QSFP-DD isn't a factor, OSFP connectors can provide alternate form factors to achieve faster data rates and manage thermal performance as their larger size provides greater airflow and cooling.

The MSA-compliant QSFP 800 and QSFP-DD 1600 feature smaller form factors and are designed for backwards compatibility with previous generations.

Each of the product families listed above includes SMT connector, BiPass and external cable solutions.

- The durable SMT Connector and Cage solutions offer superior shielding from the mating interface to the SMT tails and board to ensure 224 Gbps channel operation and lower Bit Error Rate (BER).
- BiPass cables feature standardized twinax that combines I/O with near-ASIC and backplane solutions to reduce thermal load, lower rack costs and increase design flexibility to bypass the lossy PCB.
- Direct Attach (DAC) and Active Electrical Cables (AEC) enable multiple cable configurations, optimized wire termination and Common Management Interface Specification (CMIS) support for system troubleshooting. Passive DACs are ideal for low cost, low latency applications and our retimed AECs offer superior serviceability at a lower cost compared to optics.

A COLLABORATIVE APPROACH

Leveraging the expertise of a connector provider is a critical step in product selection, qualification and scaling to production. Molex knows that a collaborative approach provides faster time to market, more accurate product selection and an optimized balance of system operational demands.

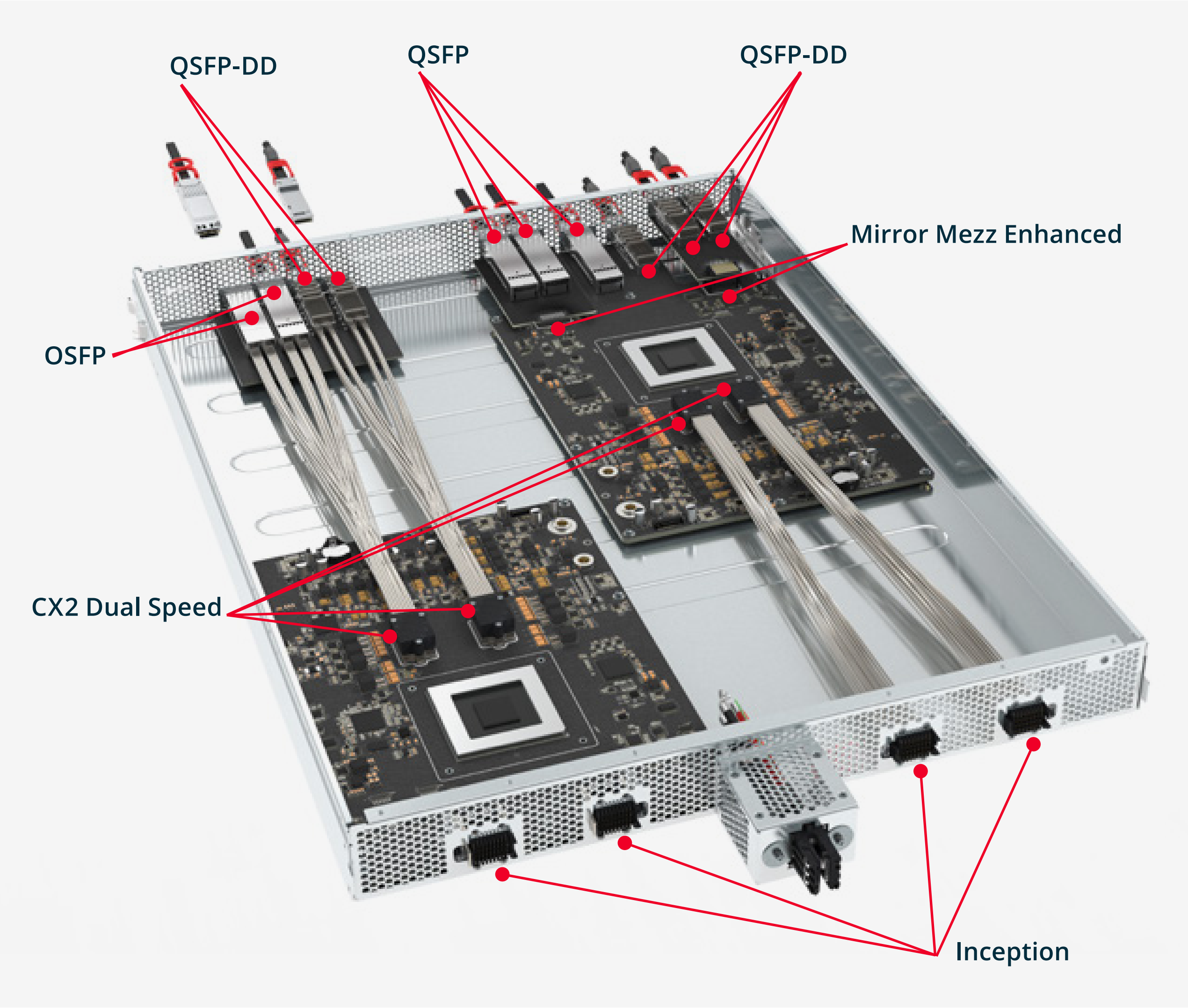
- Our engineers can provide critical advice on product selection at the beginning of a design project, which accelerates front-end engineering and physical layer design.
- Molex provides product data that can bring ECAD and MCAD together with realistic renderings, as well as signal integrity data that helps designers determine channel compliance.
- We stick with projects throughout their entire lifecycle by supporting extensible product architectures with advanced interconnect solutions.
- Molex understands the mechanical and thermal side of these products and can recommend a solution that may fit within system requirements.

ENABLING THE DATA CENTER OF TOMORROW

New technologies like generative AI, edge computing and modeling with digital twins are redefining the compute requirements in data centers. The increasing speed and volume of data being transferred between computing assets already demands solutions that can support 224G interconnects. As data-heavy applications increase, the trend of doubling data rates as compute demands grow will continue, and the industry must work across disciplines to transform data center architectures to support even faster data rates.

As each new speed limit is reached, connectors and cable systems will continue to be a critical enabler of higher bandwidth interconnects, and connector systems providers will play a major role in system design. Molex has continuously pushed the envelope and the laws of physics with more advanced connector systems supporting each data rate doubling. By leveraging the expertise of our advanced engineering team, we can codevelop next generation data center architecture to enable the most demanding applications for today and tomorrow.

Begin your journey to 224G by connecting with our expert engineering team and exploring our first-to-market, complete portfolio of 224G products.
Visit us at **molex.com/224G**.



creating connections for life

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