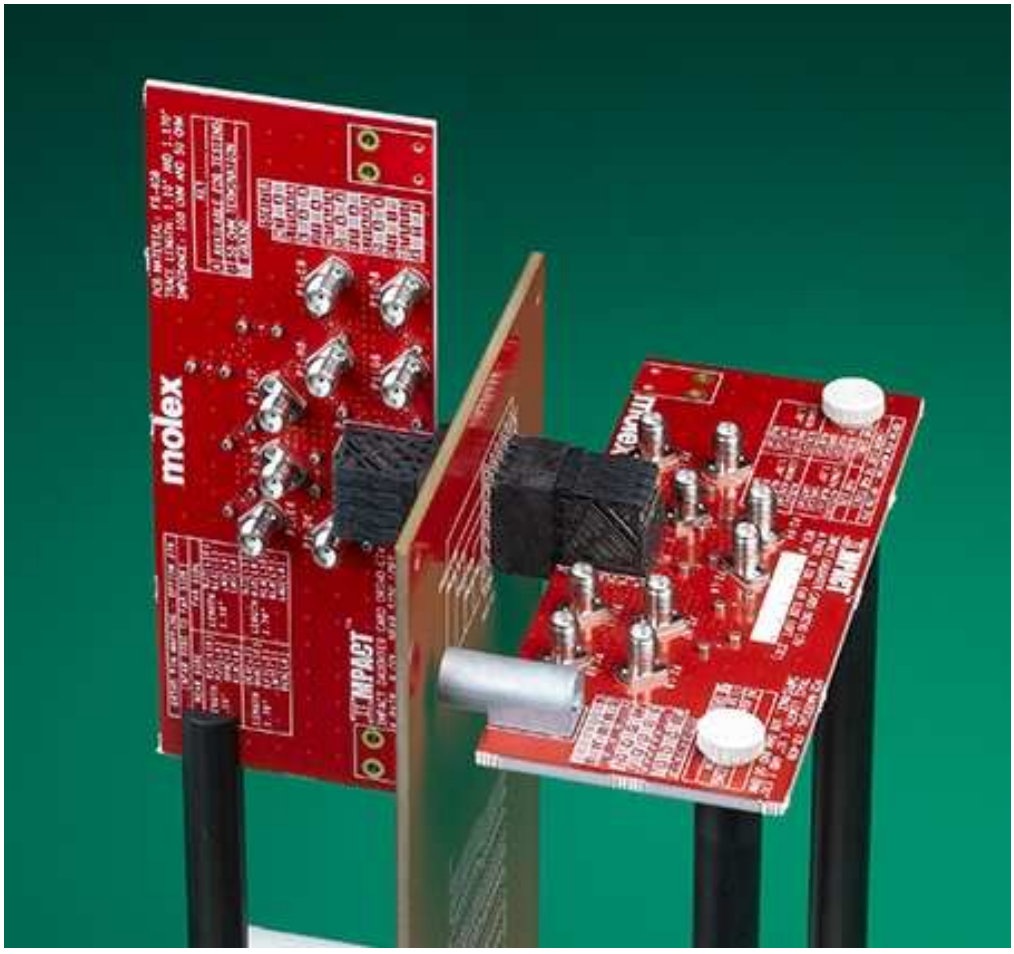
Impact™

Impact™ Orthogonal Midplane System Routing Guide



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A	EC No: **UCP2011-2515** DATE: **2011/03/08**	**IMPACT ORTHOGONAL MIDPLANE SYSTEM ROUTING GUIDE**	**1** of **17**

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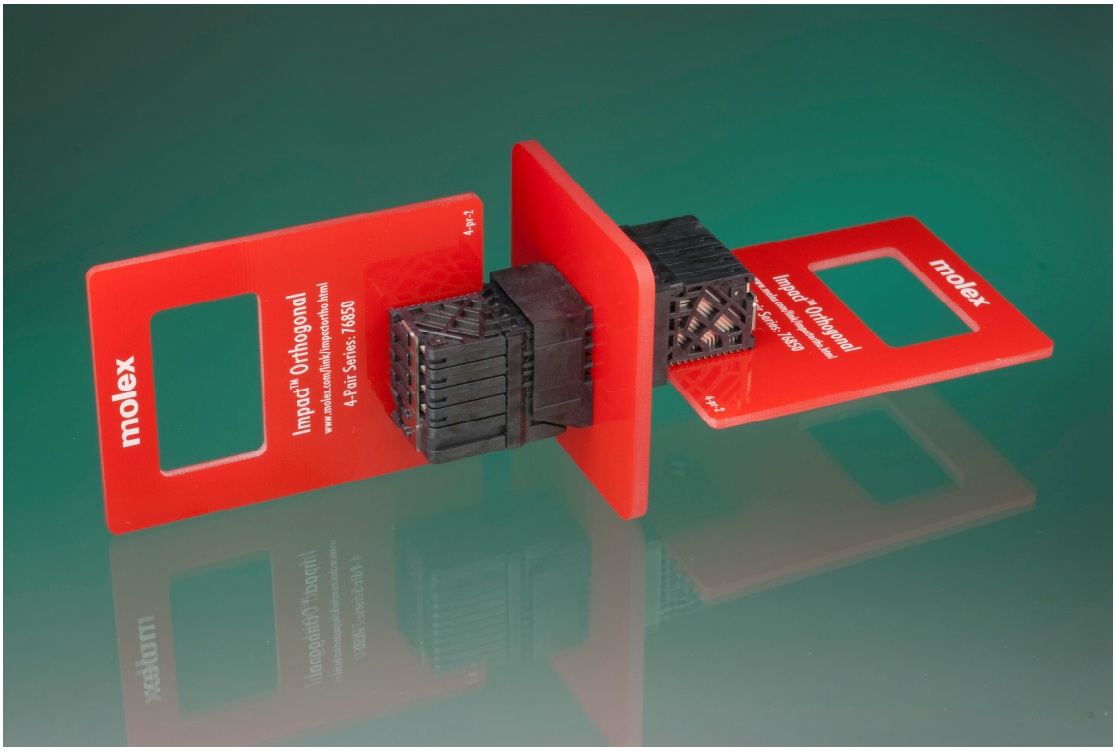
I. OVERVIEW OF THE CONNECTOR

The Impact Orthogonal midplane connector system provides data rates up to 25 Gbps and superior signal density. The Impact System's broad-edge-coupled technology enables low cross-talk and high signal bandwidth while minimizing channel performance variation across every differential pair within the system.

Molex's Impact System offers multiple compliant-pin design options on both the daughter card and backplane connectors, providing customers ultimate flexibility to optimize their designs for superior mechanical and electrical performance.

The Impact Orthogonal connector system is designed for orthogonal midplane architectures to meet the growing demands of next-generation telecommunication and data networking equipment manufacturers.



II. ROUTING STRATEGIES

A) Compliant Pin Via Constructions

The Impact connector system is available in two distinct compliant pin sizes, designed for 0.39mm diameter and 0.46mm diameter plated-thru-holes. Unlike standard Impact, the pcb hole patterns for Impact Ortho are different between the midplane and daughter card. Figure 1 illustrates the daughter card connector hole pattern. Figure 2 illustrates the midplane connector hole pattern.

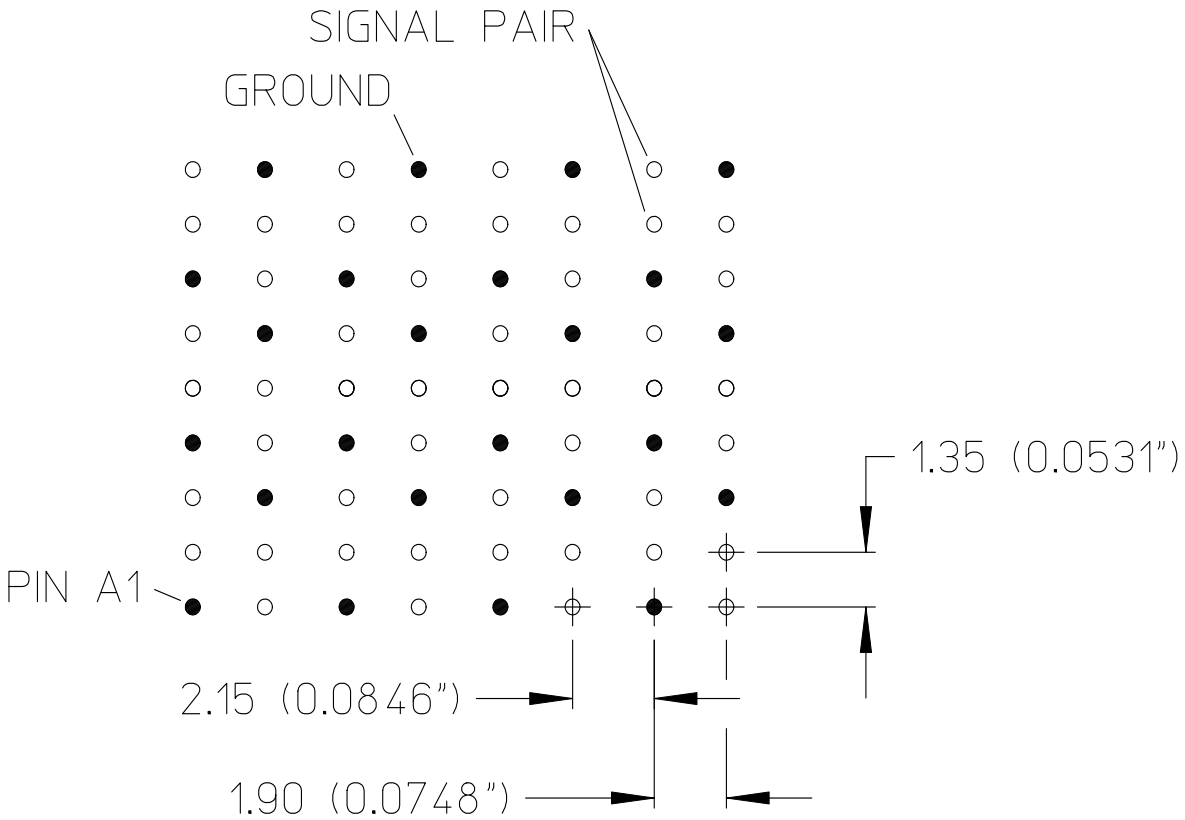


Figure 1
Daughter Card Connector Hole Pattern

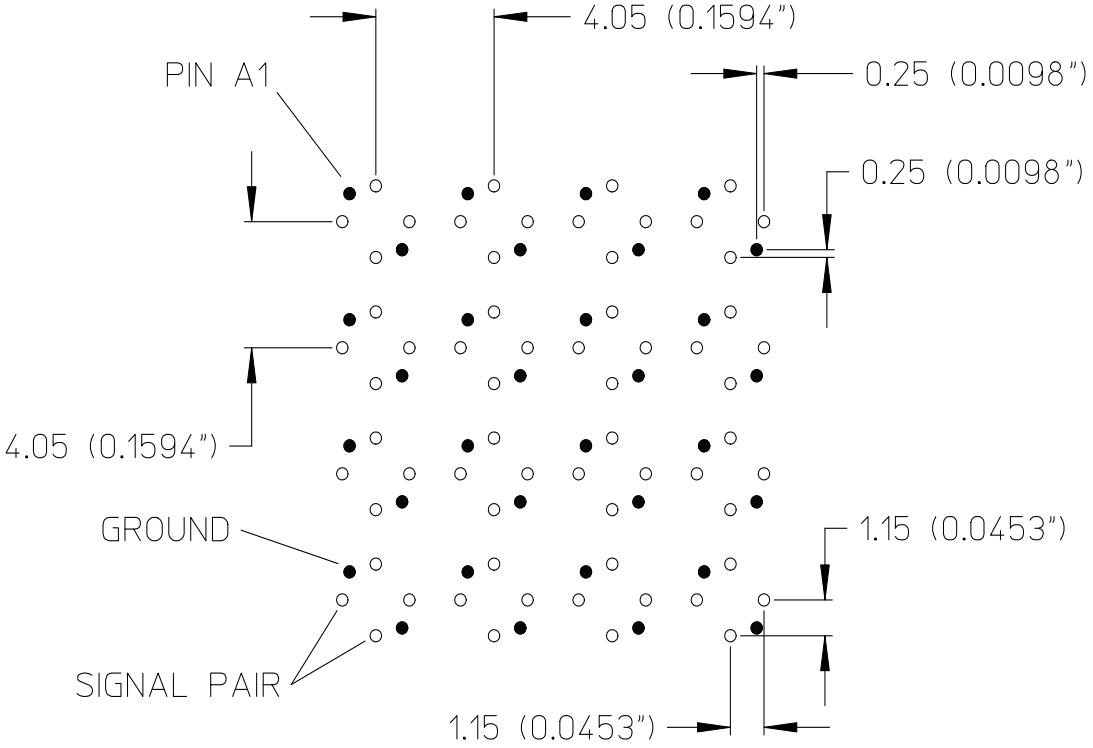


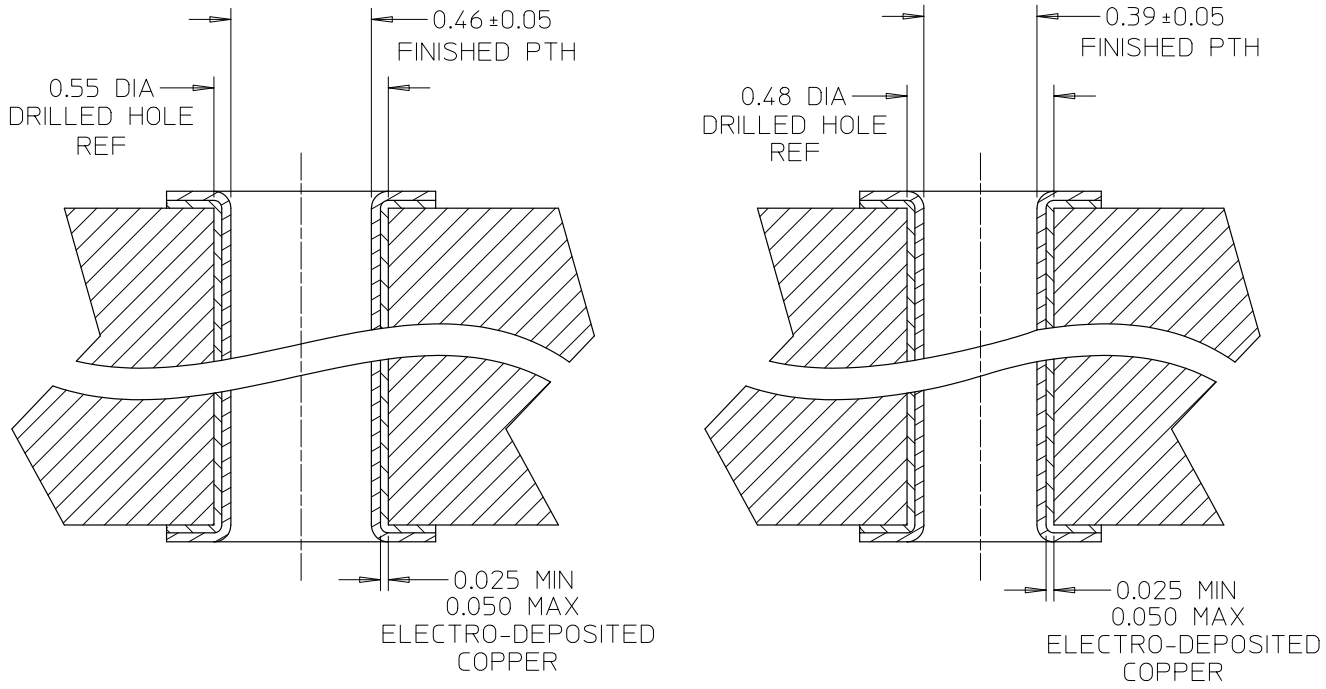
Figure 2
Backplane Connector Hole Pattern

The recommended pad stack for the two hole sizes are contained in Table A. All non-functional pads are to be removed for high speed applications.

FEATURE	0.39mm PTH NOMINAL DIA	0.46mm PTH NOMINAL DIA
Finished hole	0.39mm (15.3 mil)	0.46mm (18 mil)
Drill	0.48mm (18.9 mil)	0.55mm (21.7 mil)
Interior Pad	0.71mm (28 mil)	0.80mm (31.5 mil)
Top Layer Pad	0.80mm (31.5 mil)	0.80mm (31.5mil)
Bottom Layer Pad (MP)	0.80mm (31.5 mil)	0.80mm (31.5 mil)
Bottom Layer Pad (DC)	0.71mm (28 mil)	0.80mm (31.5 mil)
Anti-pad	See Figures 3, 4, and 7	See Figures 3, 4, and 7

Table A
Pad Stack Dimensions

Refer to the appropriate Sales Drawing for the recommended pcb thickness.



Notes:

1. The finished pcb hole size is the critical feature for proper performance of the compliant pin terminal. The reference drill sizes listed are recommended based on Molex's qualification to achieve the finished pcb hole size.
2. Depending upon the specific manufacturer's plating process, a different drill size can be used to achieve the required finished pcb hole size.
3. The typical drill hole tolerance is +/-0.013mm.

B) Transmission Line Configuration

Coupled differential strip lines are the recommended transmission lines for high speed applications. For a specific system differential impedance (i.e., 100 or 85 ohms), different trace width and spacing can be accommodated for any preferred pcb stack up configuration. Designers often consider particular common mode impedance based on factors such as skew, fabrication consistency, and density. Any particular choice of trace width and spacing ultimately affects the routing configuration within the routing channel. In high speed applications, the routing channel is a defined channel between the connector column pins.

C) Anti-pad Size - Daughtercard

For most high-speed applications, one needs to maximize the anti-pad width (between columns) and length (between rows). The width of the anti-pad is affected by the following:

1) Trace width and spacing
2) Pair to pair spacing
3) Top and bottom ground strips to trace edge spacing

The length of the anti-pad is limited by the distance and the construction of ground pin vias.
The anti-pads shown in Figure 3 are based on a 7 mil trace width and spacing and a 4 mil registration buffer (top and bottom ground strips edge to trace outer edge).

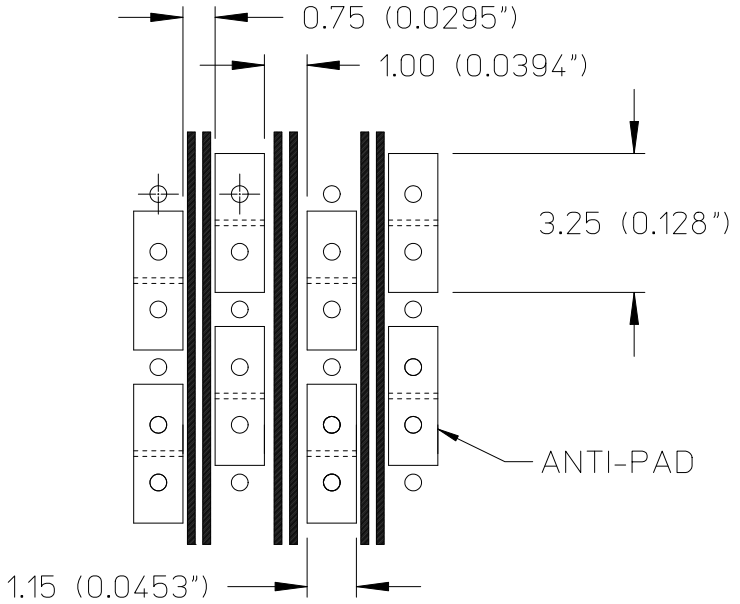


Figure 3
Daughter Card Trace Routing

D) Anti-pad Size – Midplane

For most high-speed orthogonal applications, one needs to maximize the anti-pad size. Figure 4 illustrates the recommended anti-pad size for the Impact Ortho midplane.

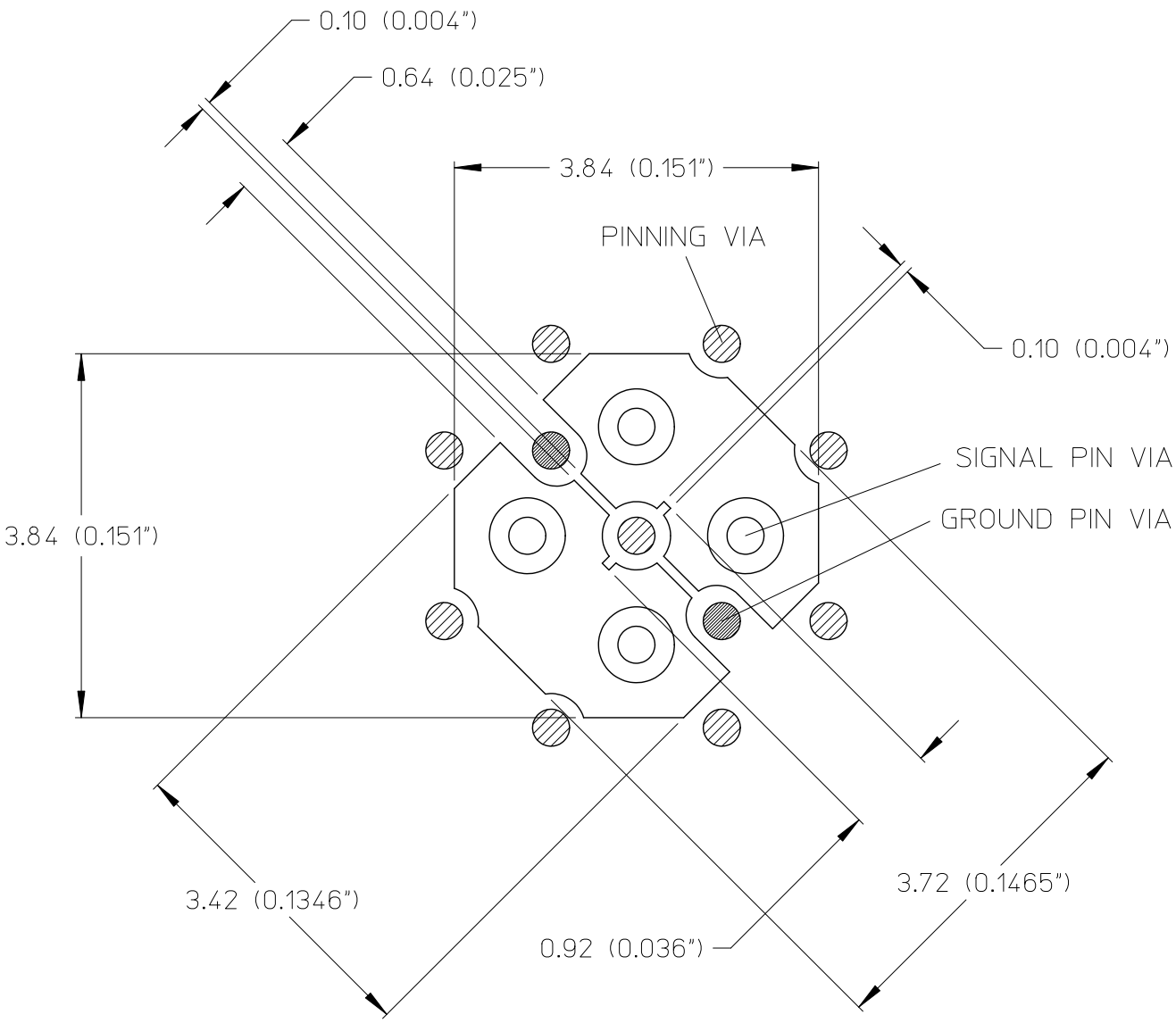


Figure 4
Midplane Anti-pad

E) Differential Trace to Signal Pad Attachment

There are several ways to connect the differential traces to their corresponding signal pads. Two possible methods are illustrated in Figures 5 and 6.

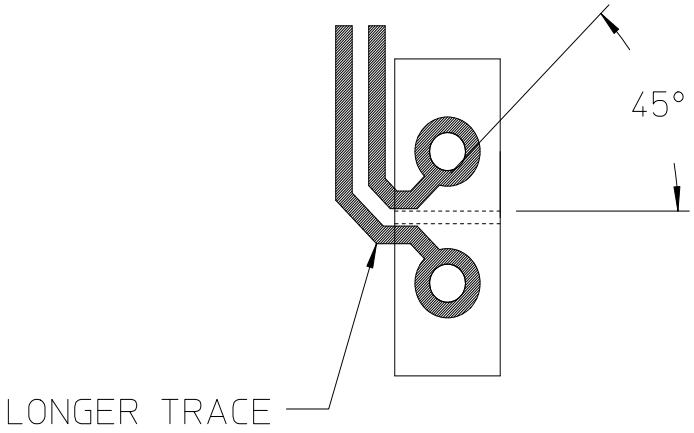


Figure 5
Standard Escape Detail (daughter card)

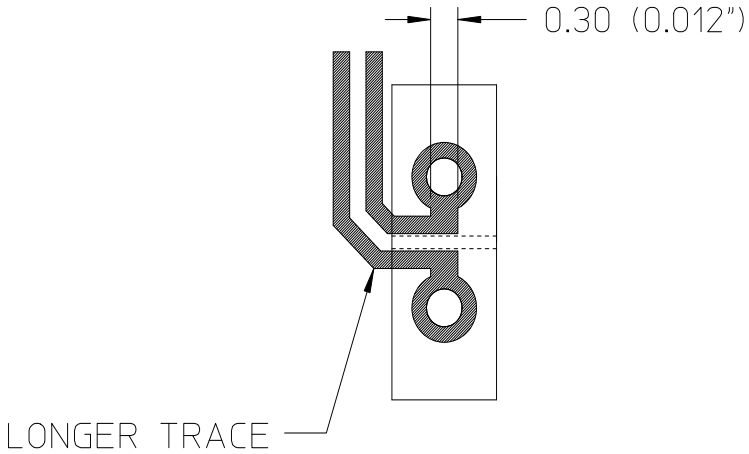


Figure 6
Flag Escape Detail (daughter card)

As seen in Figures 5 and 6, one of the traces has a longer length than the other one. This natural uneven length can be used to reduce the skew within the connector by connecting the longer trace to the shorter conductor within each differential pair of the connector. For high speed applications, it is important to design the trace configuration to compensate for the connector internal skew.

F) Routing Example - Daughtercard

It is recommended to use ground pinning vias to improve the crosstalk performance of the board. Figure 7 shows the recommended pinning vias and routing example for the Impact 3 Pair daughtercard connector. Typically, the size of the pinning vias is the same size as the connector vias.

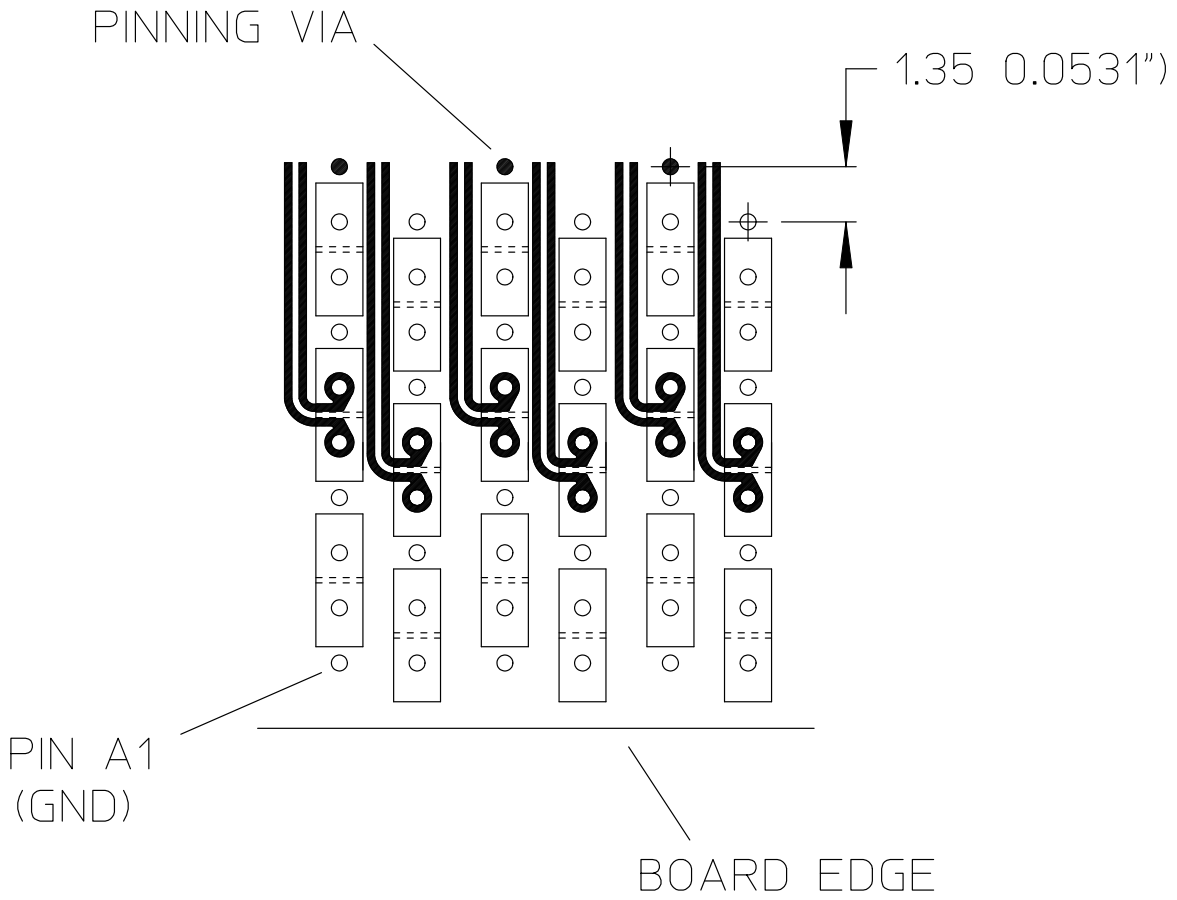


Figure 7
3 Pair x 6 Column DC Routing with recommended pinning vias

III. CROSSTALK

Crosstalk mitigation is a critical element of high speed system design. There are some simple considerations to reduce crosstalk in many systems. These include the following:

1. Separate transmit and receive transmission lines. If transmit and receive transmission lines need to be placed on the same layer, separate them with extra space. It is recommended to place them on separate routing layers.
2. Separate transmit and receive vias. Group the TX and RX differential vias in blocks in rows or columns and, if possible, separate them with slow or DC signal lines.

Tables C and D show two examples of TX and RX grouping.

	1	2	3	4	5	6	7	8
A	G	TX	G	TX	G	RX	G	RX
B	TX	TX	TX	TX	RX	RX	RX	RX
C	TX	G	TX	G	RX	G	RX	G
D	G	TX	G	TX	G	RX	G	RX
E	TX	TX	TX	TX	RX	RX	RX	RX
F	TX	G	TX	G	RX	G	RX	G
G	G	TX	G	TX	G	RX	G	RX
H	TX	TX	TX	TX	RX	RX	RX	RX
J	TX	G	TX	G	RX	G	RX	G
K	G	TX	G	TX	G	RX	G	RX
L	TX	TX	TX	TX	RX	RX	RX	RX
M	TX	G	TX	G	RX	G	RX	G

Table C
TX RX Grouping by Columns

	1	2	3	4	5	6	7	8
A	G	TX	G	TX	G	TX	G	TX
B	TX	TX	TX	TX	TX	TX	TX	TX
C	TX	G	TX	G	TX	G	TX	G
D	G	TX	G	TX	G	TX	G	TX
E	TX	TX	TX	TX	TX	TX	TX	TX
F	TX	G	TX	G	TX	G	TX	G
G	G	RX	G	RX	G	RX	G	RX
H	RX	RX	RX	RX	RX	RX	RX	RX
J	RX	G	RX	G	RX	G	RX	G
K	G	RX	G	RX	G	RX	G	RX
L	RX	RX	RX	RX	RX	RX	RX	RX
M	RX	G	RX	G	RX	G	RX	G

Table D
TX RX Grouping by Rows (separated by defined grounds)

For orthogonal midplane architectures, it is especially important to optimize the midplane board, as it is a critical element of the system design. For this reason, it is recommended to use ground pinning vias to improve the crosstalk performance of the board. Figure 8 details the recommended pinning via arrangement for Impact. Typically, the size of the pinning vias is the same as the size of the connector vias. Please note that the perimeter of the standard anti-pad (shown in Figure 4) is modified to accommodate the pads required by the ground pinning vias.

While the addition of pinning vias and air holes can add complexity to the midplane pattern (see Figure 9), the channel noise reduction and impedance improvement is significant.

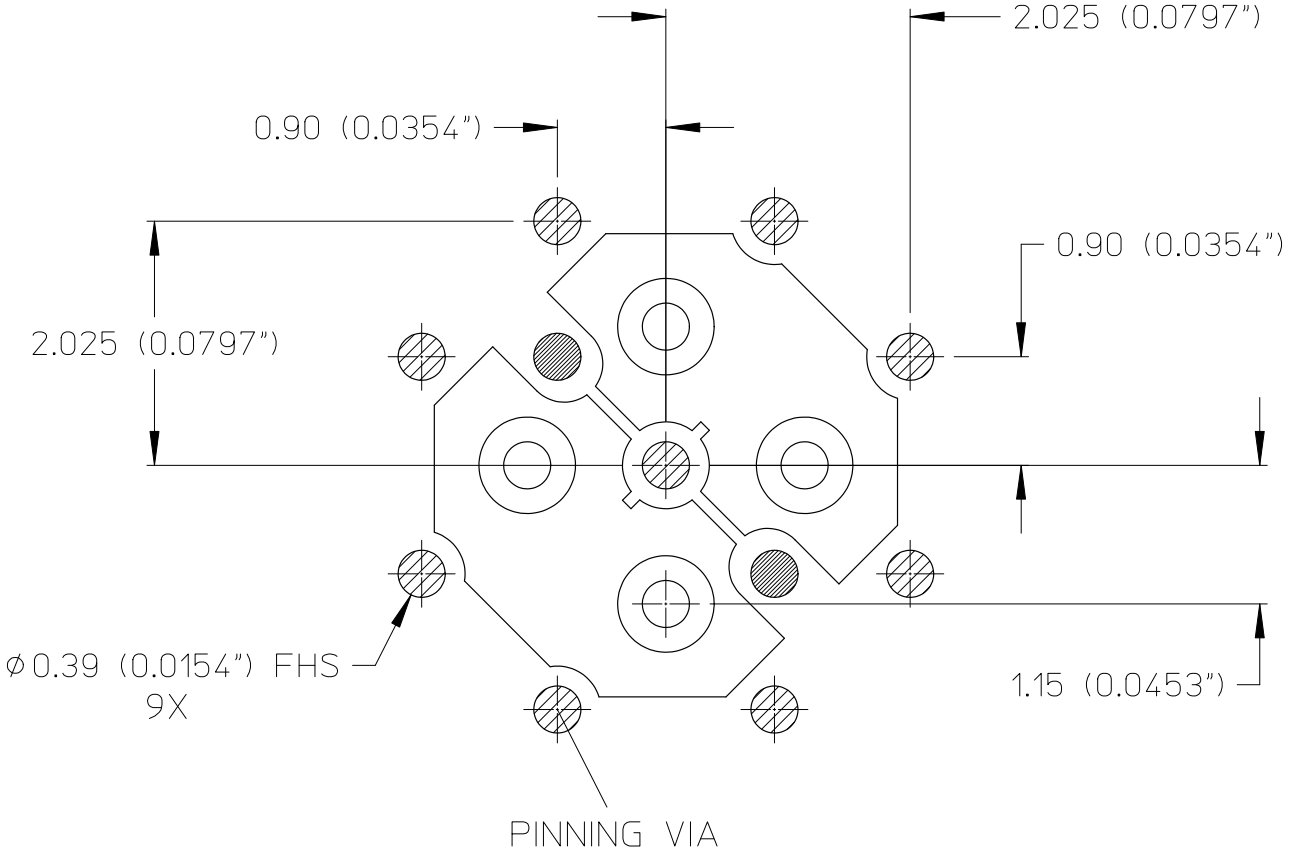


Figure 8

Pinning Vias for Optimized SI Performance
(Pinning Via Dimensions)

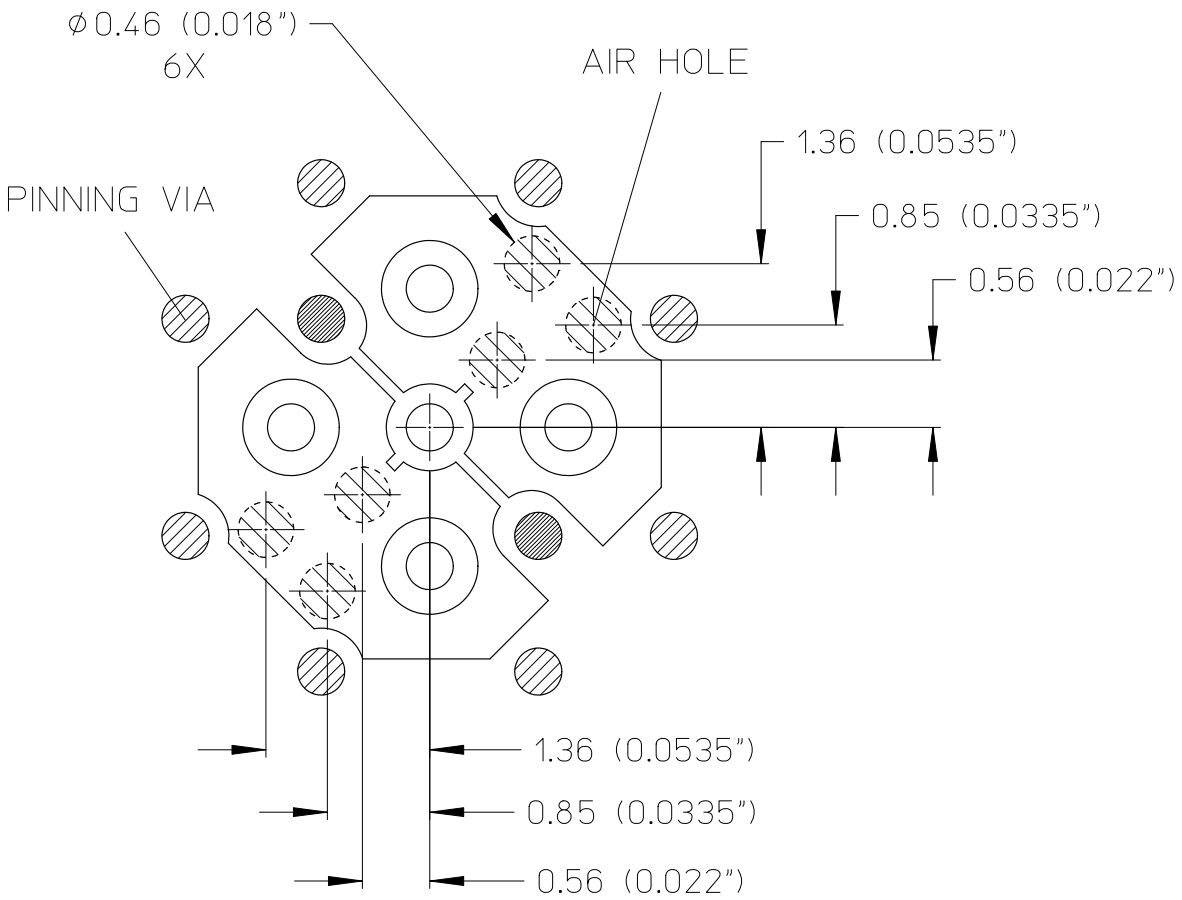


Figure 9

Optional Air Holes for Optimized Impedance Performance
(Air Hole Dimensions)

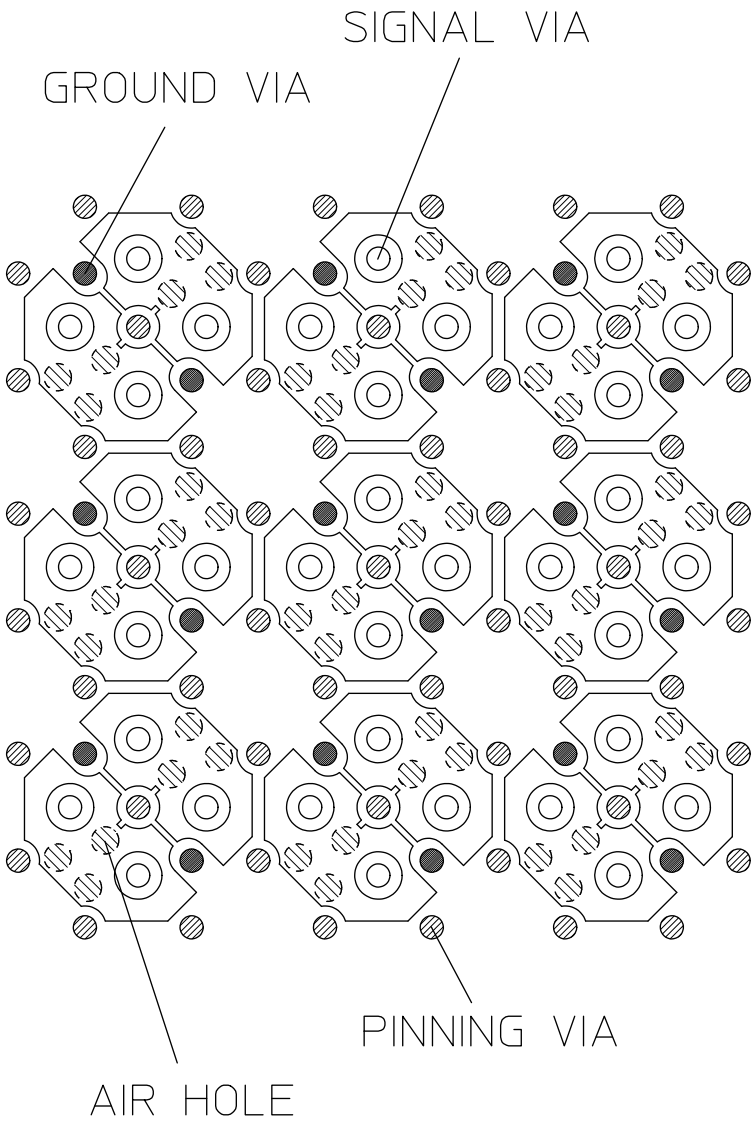


Figure 10

3 Pair, 6 Column – Optimized Midplane Pattern
(Top and Bottom Ground Layers)

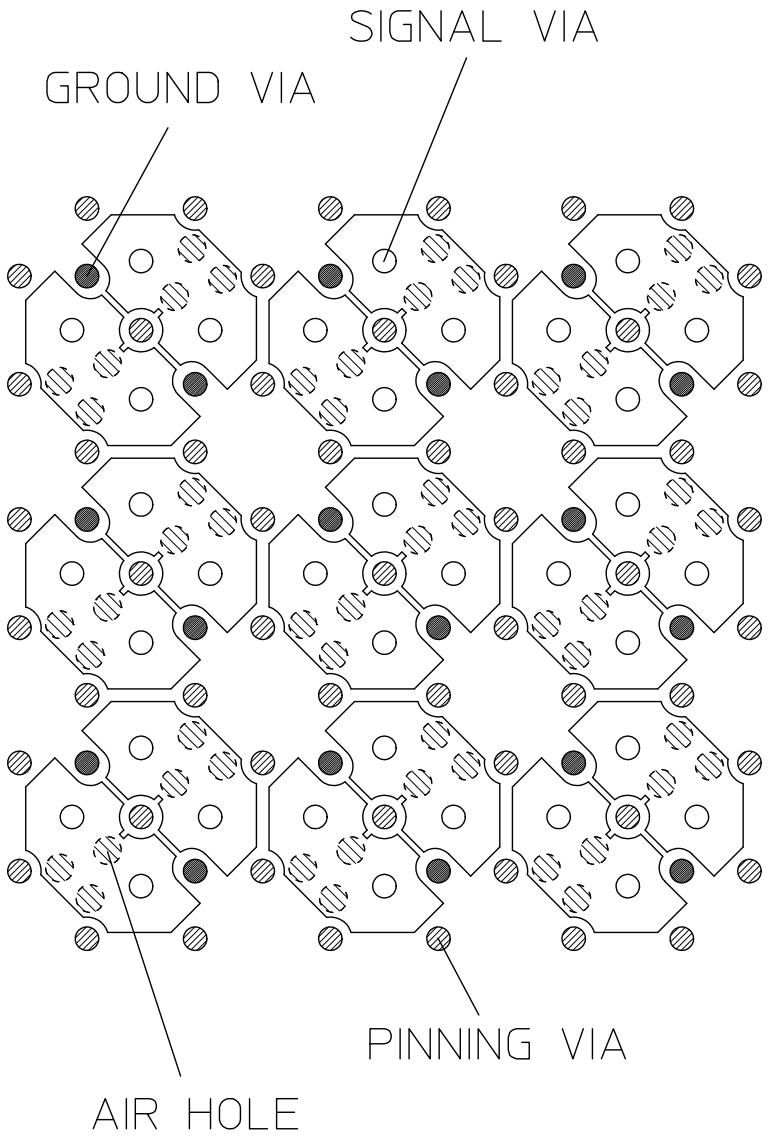


Figure 11

3 Pair, 6 Column – Optimized Midplane Pattern
(Internal Ground Layers)

IV. BACK DRILLING

For high speed signals, it may be necessary to remove excess via stub below the pcb signal layer. This is accomplished by backdrilling the plated via with a larger diameter drill to remove the undesirable excess via, The Impact compliant pin design allows for backdrilling to within 1mm of the top surface of the pcb. For orthogonal midplane applications, backdrilling is only possible on the daughter cards, as the midplane vias are shared.

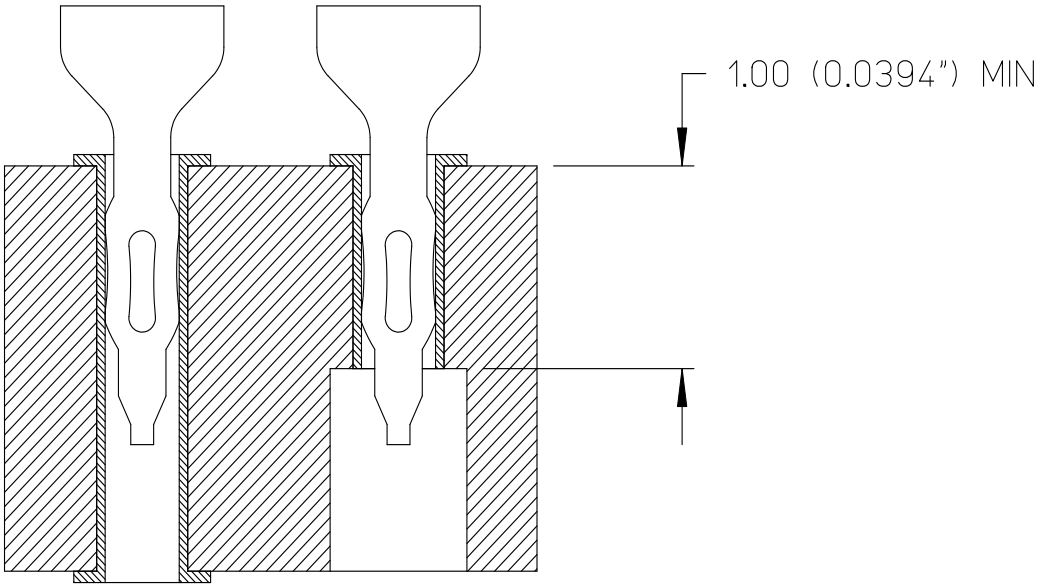


Figure 12
Backdrill Specification